Disclosure Amendments

On page 1, in the paragraph beginning at line 30:

In the unachievable ideal case, the switches represent zero-ohm, zero-length wires when closed and infinite resistance connections when opened. Since most FPIDs are based on silicon MOSFET devices, however, the switches do not achieve the ideal behavior. FIG. 2 illustrates the various representations of the switch in an FPID. FIG.2a is the simplified symbolic representation. FIG. 2b is the familiar standard symbolic representation. Figures 2c and 2d represent the n-channel MOSFET and CMOS (n-channel plus p-channel) transmission gate structures respectively, which closely represent the actual switch structures in FPID devices. FIG. 3 provides a more physically accurate representation of an n-channel MOSFET. FIG. 3b illustrates the formation of an inversion channel between the drain and source, resulting in a conductive path, the situation more closely representing the closure of an FPID switch. The switch actually behaves more like ~~a~~ the resistor shown in Fig. 3c, a fact very important to the principle behind the present invention.

On page 6, after line 12 (in the section titled "Brief Description of the Drawings"):

FIG. 3 illustrates the transformation of an n-channel MOSFET using an inversion channel.

On page 6, after line 23 (in the section titled "Brief Description of the Drawings"):

FIG. 7 illustrates networks of switches configured to present parasitic resistances.

On page 7, in the paragraph beginning at line 14 (in the section titled "Brief Description of the Drawings"):

FIG. 13 shows a finite difference mesh ~~(11a)~~ (13a) that is too large to fit onto one FPID device and ~~(11b)~~ (13b) shows how this mesh might be sectioned into four segments.